Fig 1

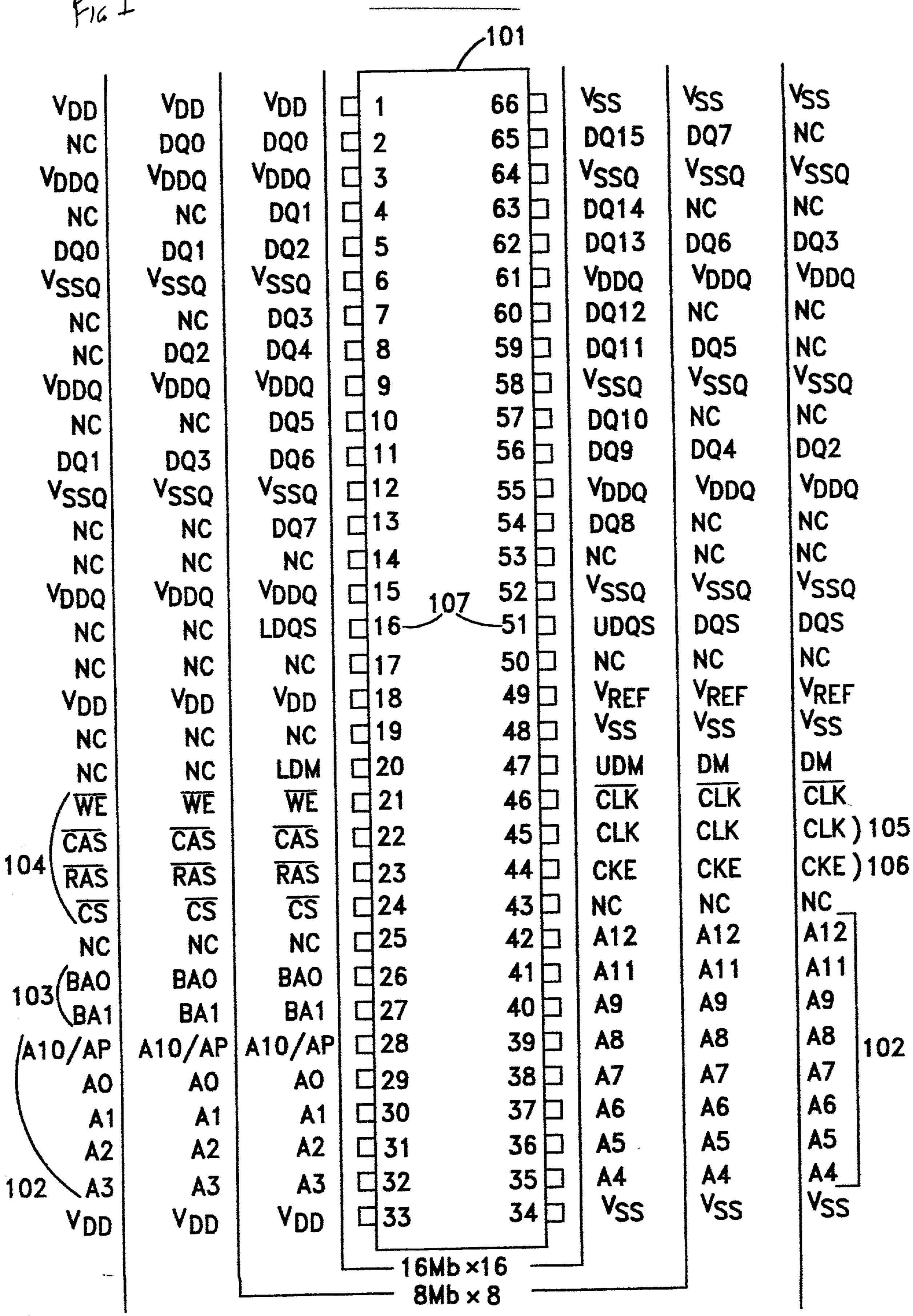

101
VDD VDD VDD 1 66 VSS VSS VSS
NC DQ0 DQ0 2 65 DQ15 DQ7 NC
VDDQ VDDQ VDDQ 3 64 VSSQ VSSQ VSSQ
NC NC DQ1 4 63 DQ14 NC NC
DQ0 DQ1 DQ2 5 62 DQ13 DQ6 DQ3
VSSQ VSSQ VSSQ 6 61 VDDQ VDDQ VDDQ
NC NC DQ3 7 60 DQ12 NC NC
NC DQ2 DQ4 8 59 DQ11 DQ5 NC
VDDQ VDDQ VDDQ 9 58 VSSQ VSSQ VSSQ
NC NC DQ5 10 57 DQ10 NC NC
DQ1 DQ3 DQ6 11 56 DQ9 DQ4 DQ2
VSSQ VSSQ VSSQ 12 55 VDDQ VDDQ VDDQ
NC NC DQ7 13 54 DQ8 NC NC
NC NC NC 14 53 NC NC NC
VDDQ VDDQ VDDQ 15 52 VSSQ VSSQ VSSQ
NC NC LDQS 16 107 51 UDQS DQS DQS
NC NC NC 17 50 NC NC NC
VDD VDD VDD 18 49 VREF VREF VREF
NC NC NC 19 48 VSS VSS VSS
NC NC LDM 20 47 UDM DM DM
WE WE WE 21 46 CLK CLK CLK
104 CAS CAS CAS 22 45 CLK CLK CLK 105
RAS RAS RAS 23 44 CKE CKE CKE 106
CS CS CS 24 43 NC NC NC
NC NC NC 25 42 A12 A12 A12
103 BA0 BA0 BA0 26 41 A11 A11 A11
BA1 BA1 BA1 27 40 A9 A9 A9
A10/AP A10/AP A10/AP 28 39 A8 A8 A8 102
A0 A0 A0 29 38 A7 A7 A7
A1 A1 A1 30 37 A6 A6 A6
A2 A2 A2 31 36 A5 A5 A5
102 A3 A3 A3 32 35 A4 A4 A4
VDD VDD VDD 33 34 VSS VSS VSS
16Mb ×16
8Mb × 8

FIG 24

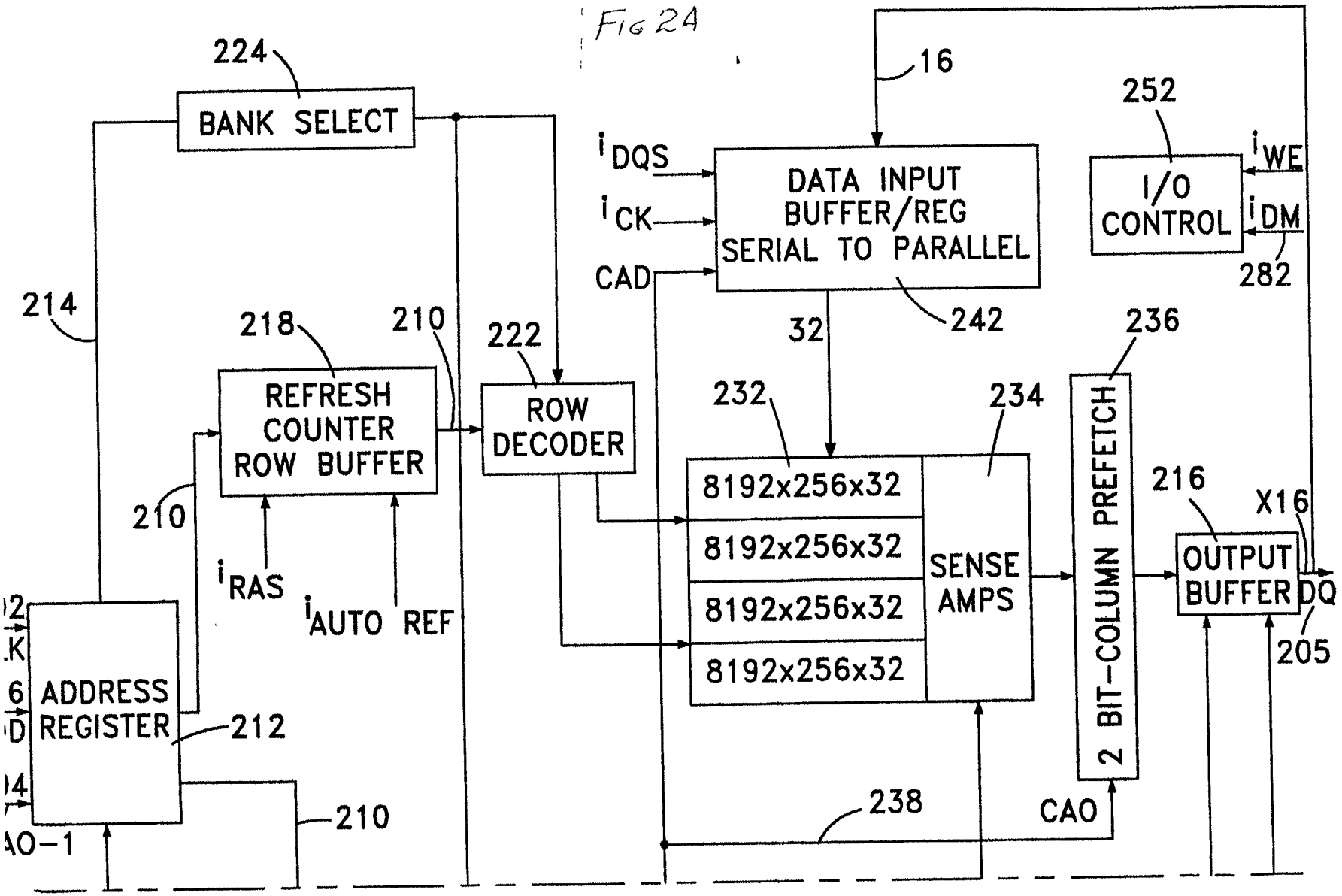

224
BANK SELECT
16
252
I/O CONTROL
iWE
iDM
282
iDQS
iCK
CAD
DATA INPUT BUFFER/REG SERIAL TO PARALLEL
242
32
214
218
210
222
REFRESH COUNTER ROW BUFFER
ROW DECODER
232
234
236
8192x256x32
8192x256x32
8192x256x32
8192x256x32
SENSE AMPS
2 BIT-COLUMN PREFETCH
216
X16
OUTPUT BUFFER
DQ
205
iRAS
iAUTO REF
ADDRESS REGISTER
212
210
238
CAO

FIG 2B

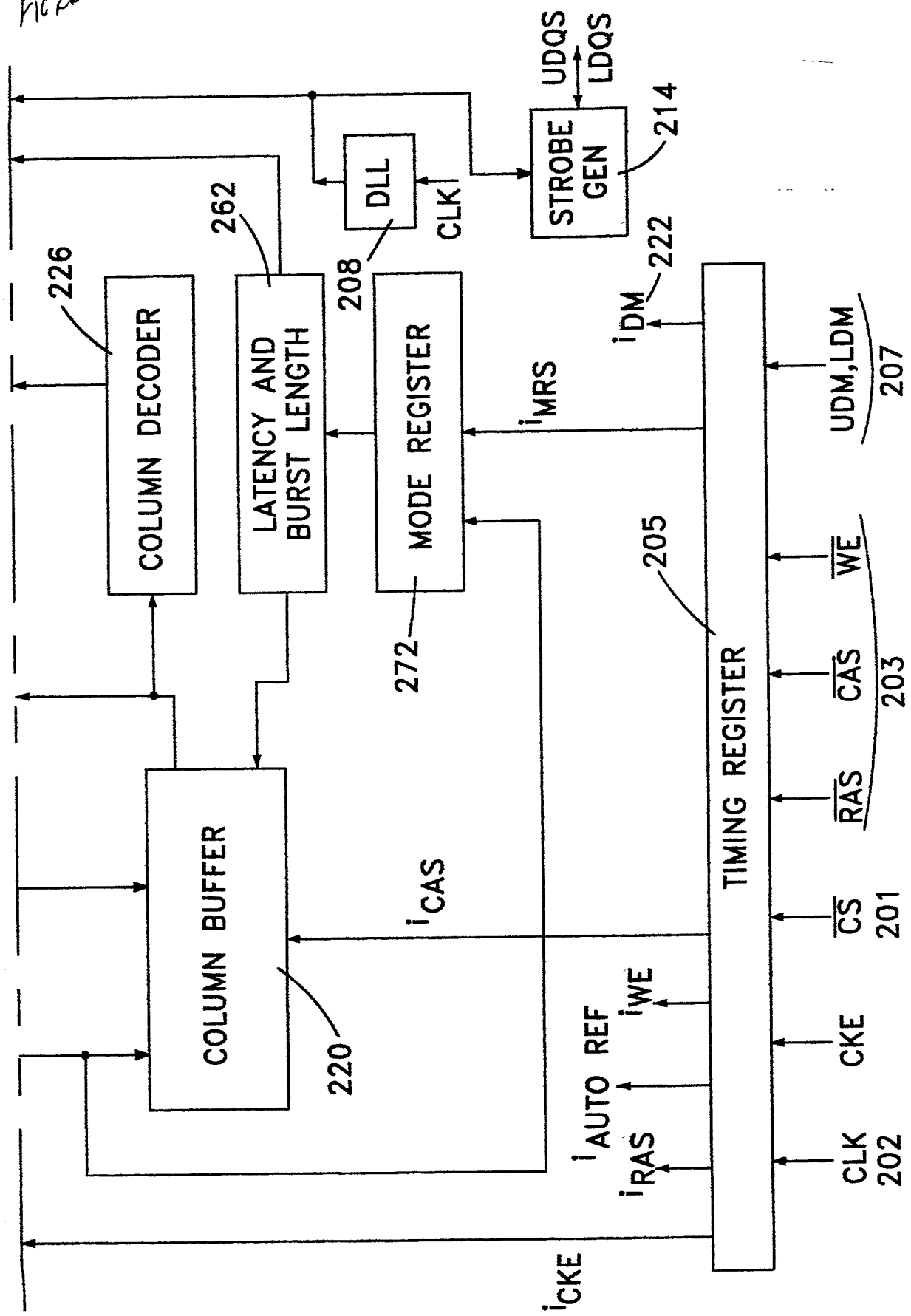

UDQS
LDQS
STROBE GEN
214
DLL
CLK
208
262
226
COLUMN DECODER
LATENCY AND BURST LENGTH
MODE REGISTER
272
i_{DM}
222
i_{MRS}
UDM,LDM
207
205
TIMING REGISTER
WE
CAS
RAS
203
CS
201
COLUMN BUFFER
220
i_{CAS}
i_{WE}
$i_{AUTO\ REF}$
i_{RAS}
CKE
CLK
202
i_{CKE}

FIG 3

OPERATION	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	BA_0 BA_1	A_{10}	A_0 A_9 A_{11}	MNE	NOTES
DEVICE DESELECT	H	X	H	X	X	X	X	X	X	X	INHBT	
NO OPERATION	H	X	L	H	H	H	X	X	X	X	NOP	
LOAD MODE REGISTER MODE OR EXTENDED MODE REGISTER	H	X	L	L	L	L	X	OP CODE			MRS/EMRS	1
ROW ACTIVATE	H	X	L	L	H	H	X	BS	ROW ADDRESS		ACT	2
READ	H	X	L	H	L	H	X	BS	L	COL	RD	3
READ W/ AUTO PRECHARGE	H	X	L	H	L	H	X	BS	H	COL	RAP	3
WRITE	H	X	L	H	L	L	V	BS	L	COL	WR	3,4
WRITE W/ AUTO PRECHARGE	H	X	L	H	L	L	V	BS	H	COL	WAP	3,4
BURST STOP	H	X	L	H	H	L	X	X	X	X	BST	5
PRECHARGE SINGLE BANK	H	X	L	L	H	L	X	BS	L	X	PRE	
PRECHARGE ALLBANKS	H	X	L	L	H	L	X	X	H	X	PREALL	
AUTO REFRESH	H	H	L	L	L	H	X	X	X	X	REF	1
SELF REFRESH ENTRY	H	L	L	L	L	H	X	X	X	X	SR(ENTRY)	1
SELF REFRESH EXIT	L	H	H	X	X	X	X	X	X	X	SR(EXIT)	
	L	H	L	H	H	H	X	X	X	X		
POWER DOWN MODE (ENTRY)	H	L	H	X	X	X	X	X	X	X	PDN(ENTRY)	
	H	L	L	H	H	H	X	X	X	X		
POWER DOWN MODE (EXIT)	L	H	X	X	X	X	X	X	X	X	PDN(EXIT)	

1 SHOULD BE ISSUED ONLY AFTER BOTH BANKS ARE DEACTIVATED (PREALL COMMAND)
2 SHOULD BE ISSUED ONLY AFTER THE CORRESPONDING BANK HAS BEEN DEACTIVATED
3 SHOULD BE ISSUED AFTER THE CORRESPONDING BANK HAS BEEN ACTIVATED
4 ANY VALUED WRITE CYCLE APPLIED TO THE SLECTED BANK/ROW WILL BE MASKED ACCORDING TO THE DM 5 SHOULD BE ISSUED ONLY DURING READ BURST CYCLE

Fig 4A

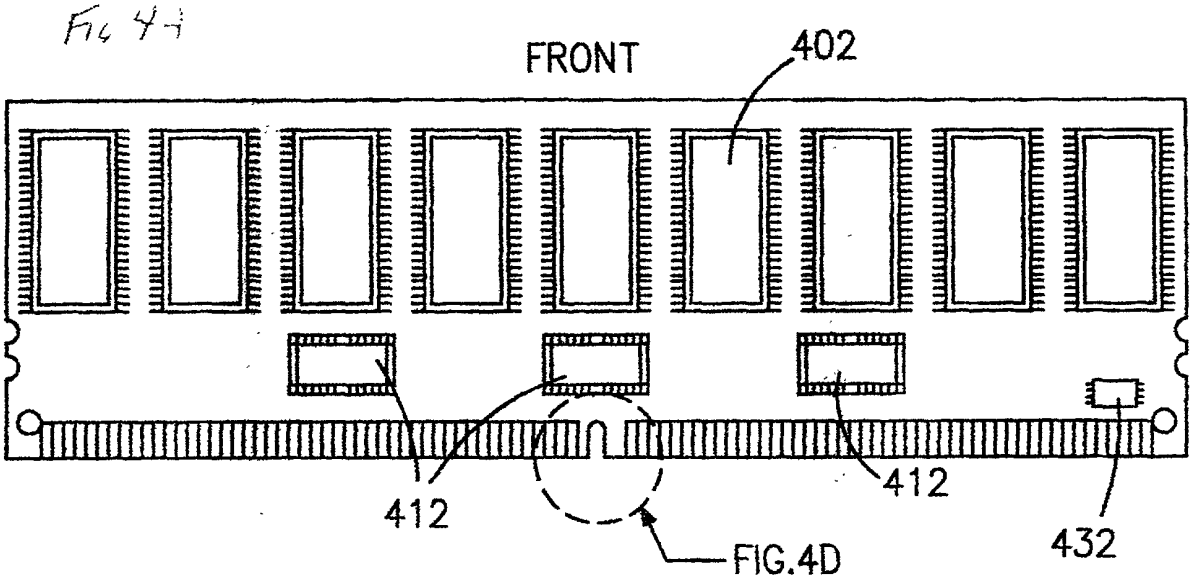
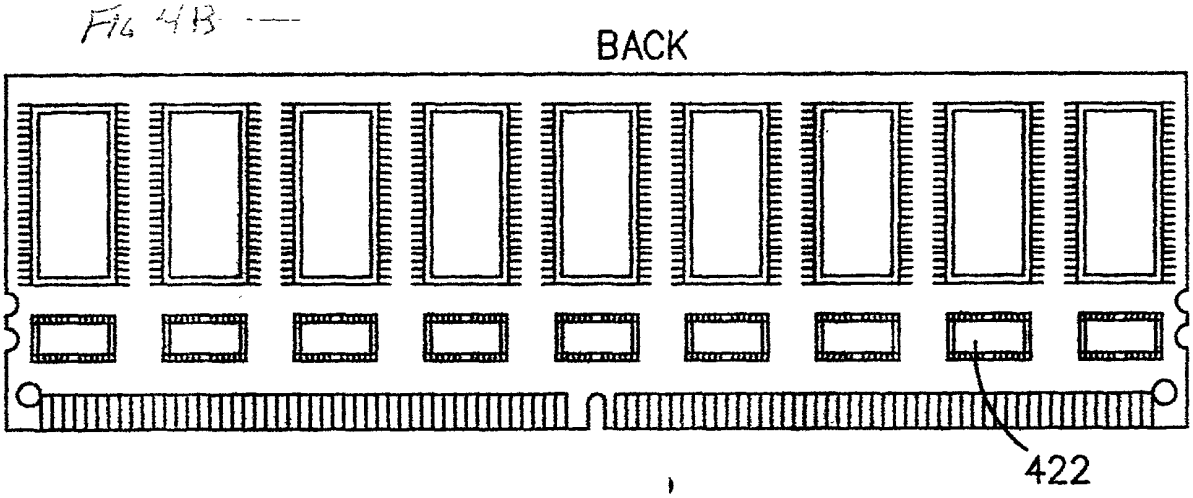


Fig 4B



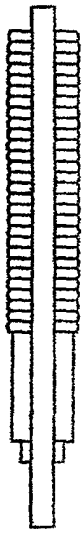


Fig 4C

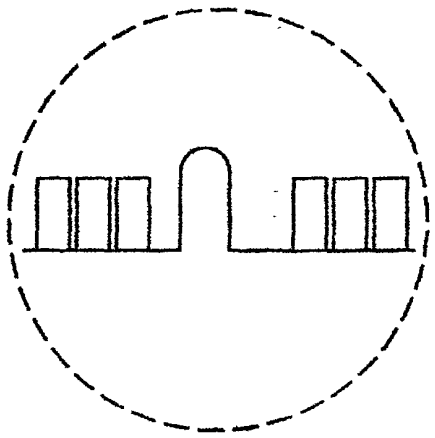


Fig 4D

FIG 5A

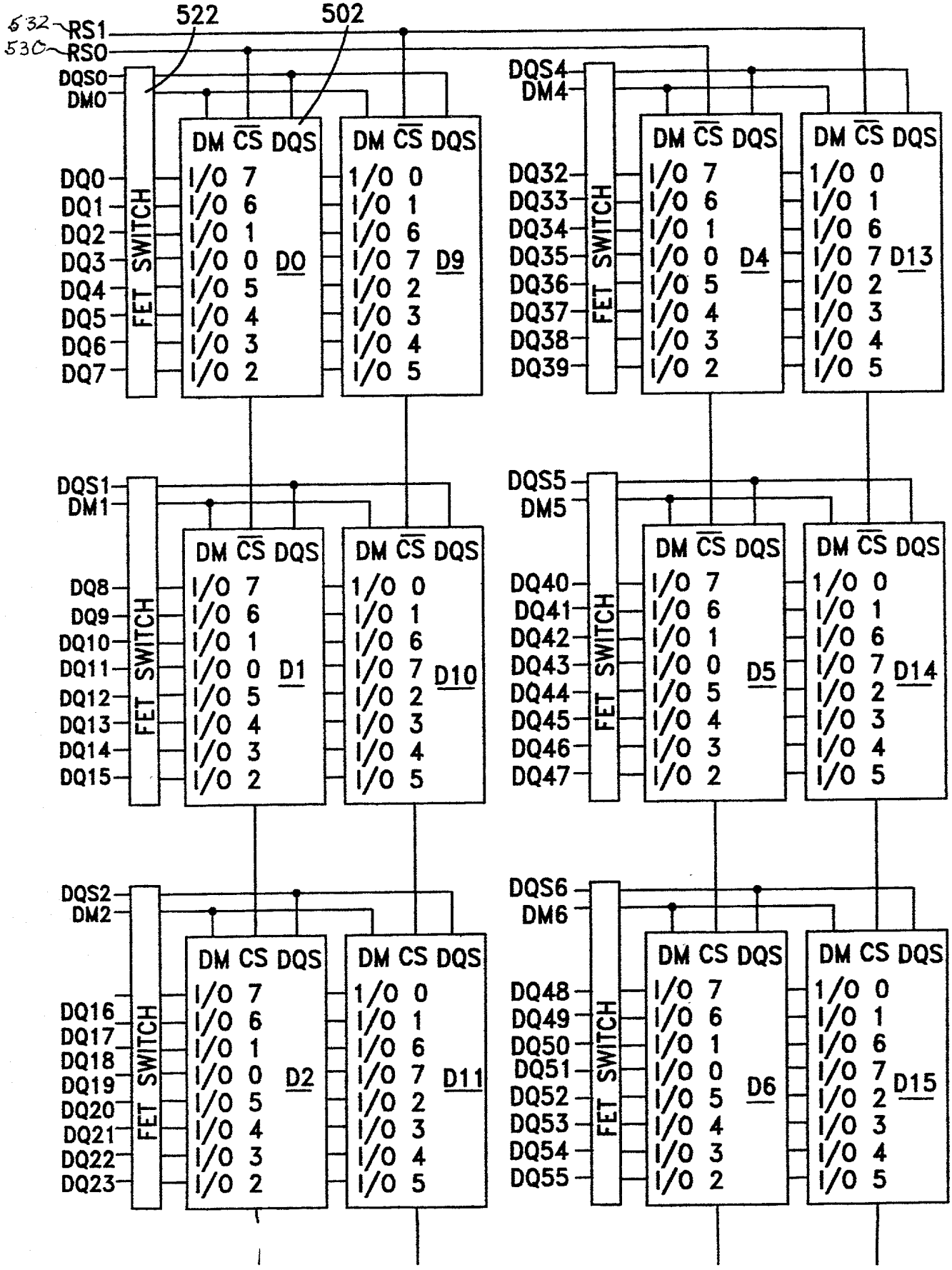

522
502
632
RS1
530
RS0
DQS0
DM0
FET SWITCH
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DM CS DQS
I/O 7
I/O 6
I/O 1
I/O 0
I/O 5
I/O 4
I/O 3
I/O 2
D0
1/O 0
I/O 1
I/O 6
I/O 7
I/O 2
I/O 3
I/O 4
I/O 5
D9
DQS4
DM4
DQ32
DQ33
DQ34
DQ35
DQ36
DQ37
DQ38
DQ39
D4
D13
DQS1
DM1
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
D1
D10
DQS5
DM5
DQ40
DQ41
DQ42
DQ43
DQ44
DQ45
DQ46
DQ47
D5
D14
DQS2
DM2
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
D2
D11
DQS6
DM6
DQ48
DQ49
DQ50
DQ51
DQ52
DQ53
DQ54
DQ55
D6
D15

FIG 5B

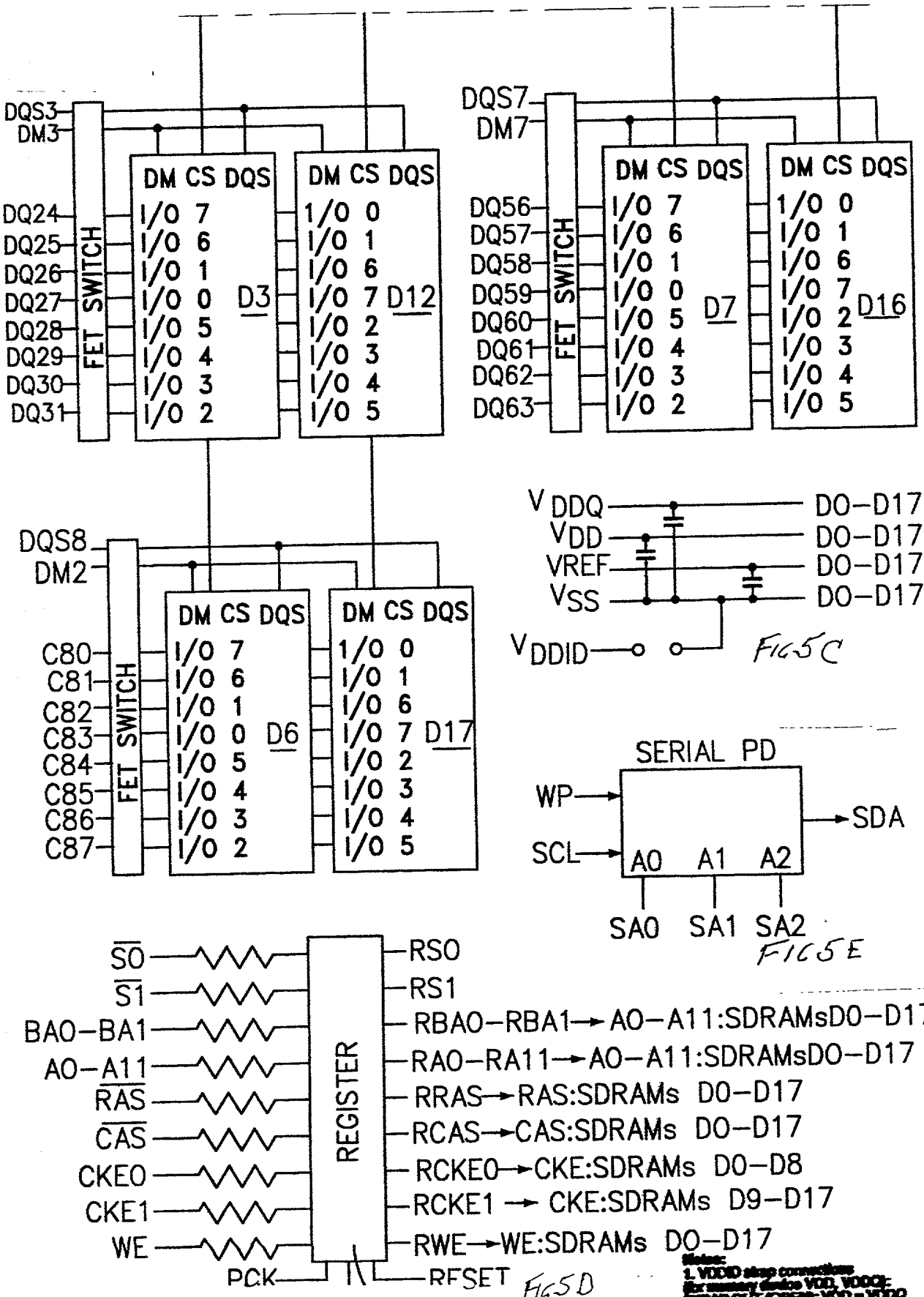


FIG 5C

FIG 5E

FIG 5D

Notes:
1. VDDID strap connections
(for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD = VDDQ
2. See FET switch detail for more information

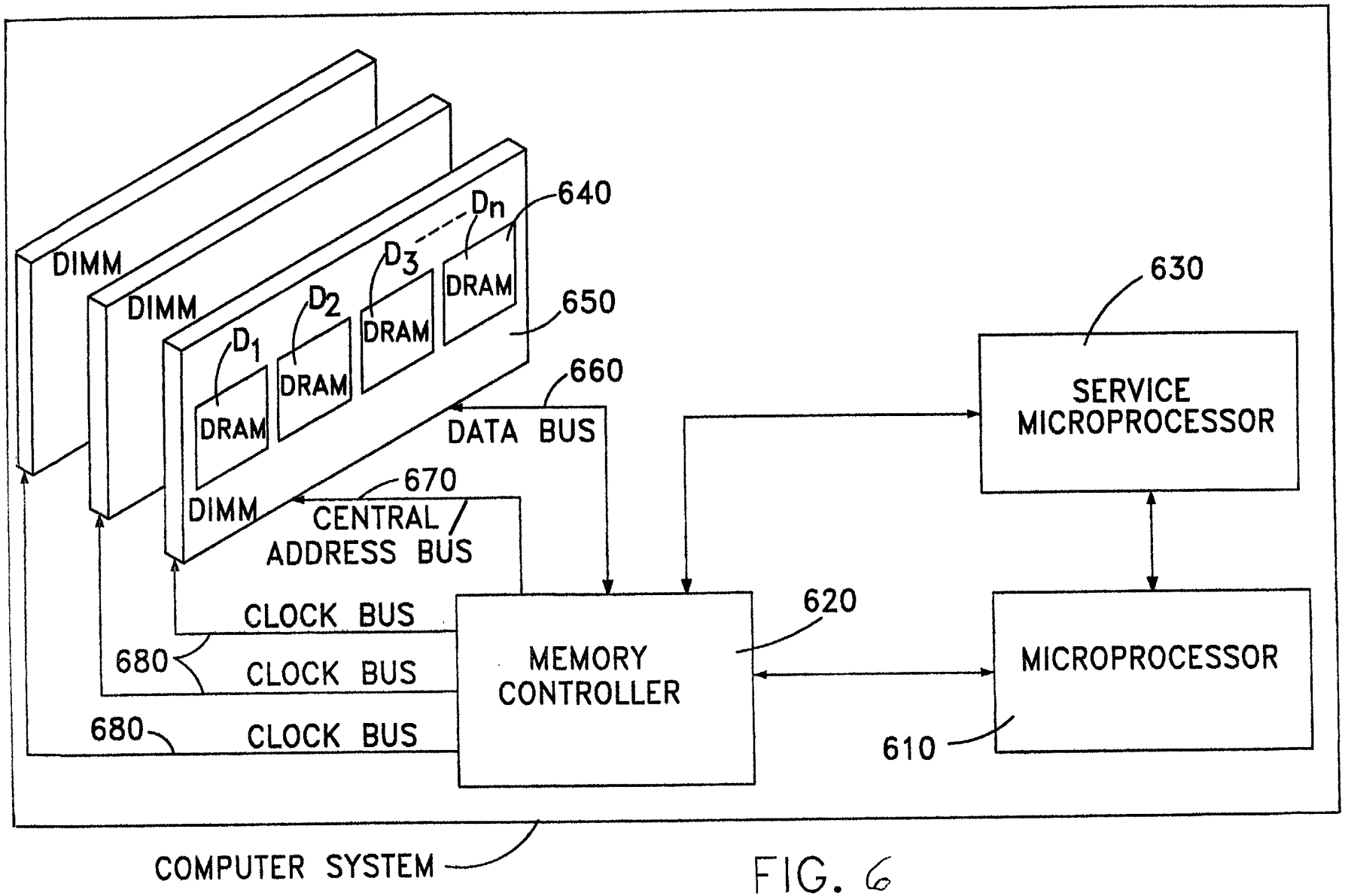


FIG. 6

FIG 7A

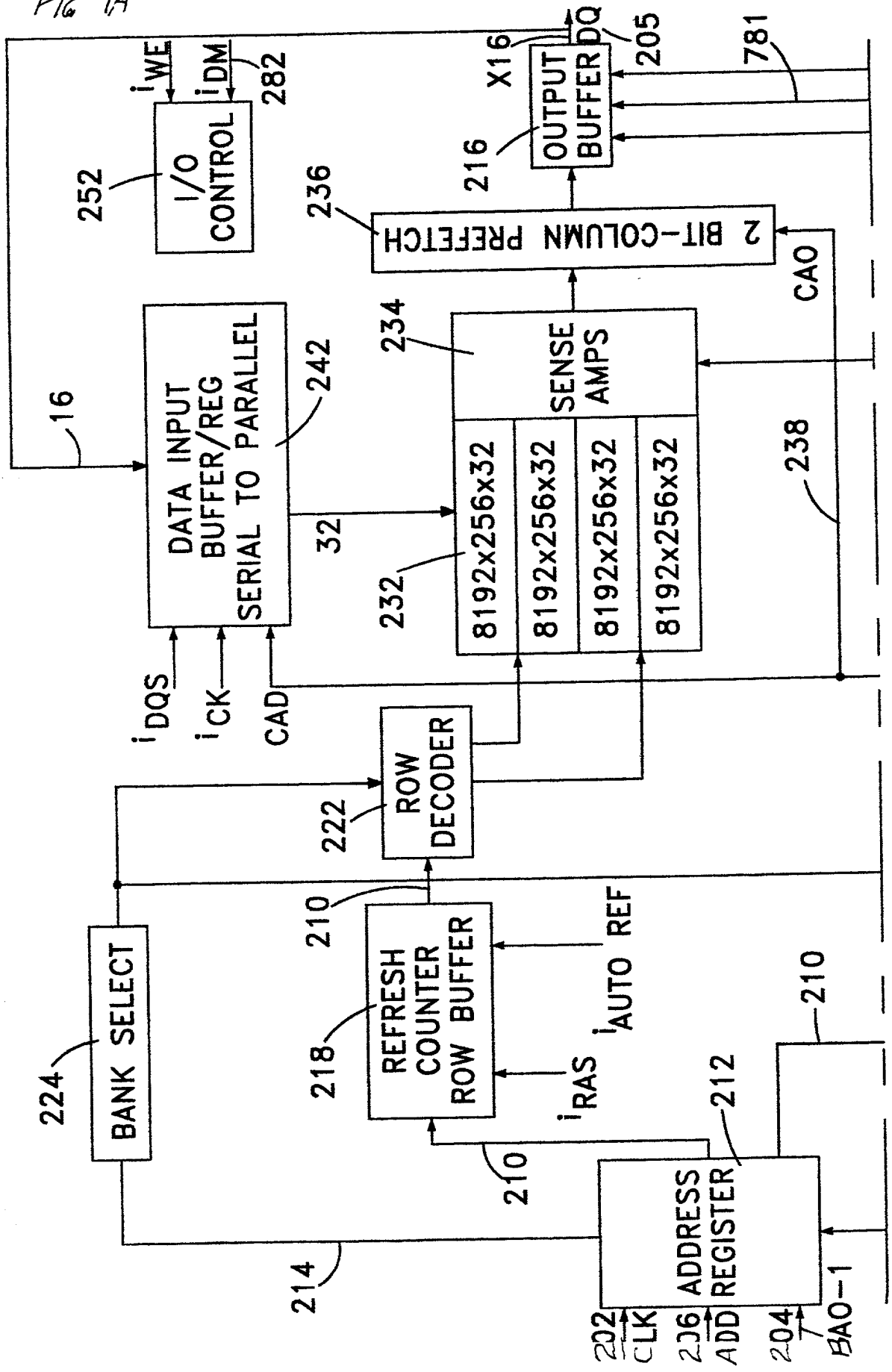
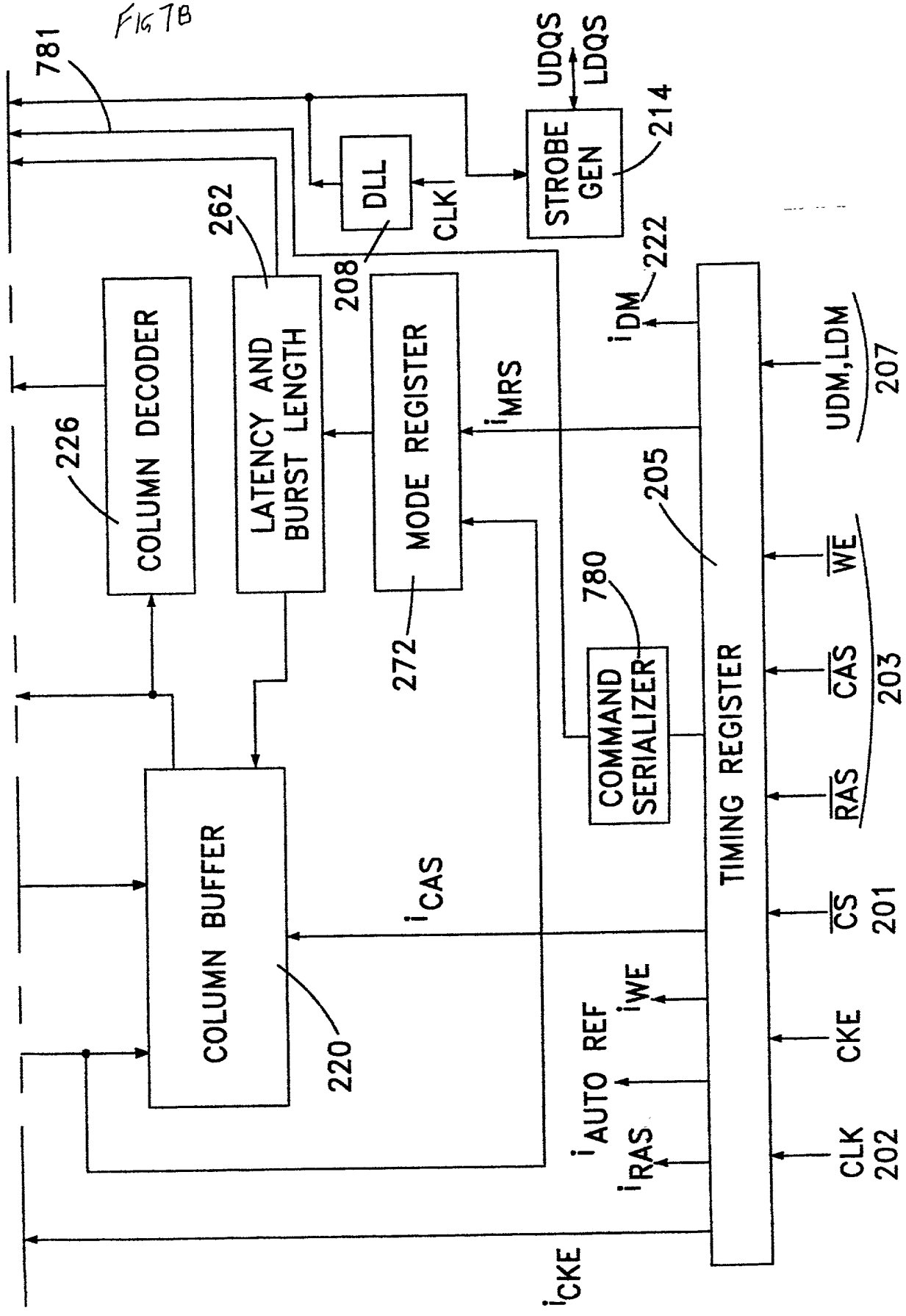

i WE
i DM
282
I/O CONTROL
252
X16
OUTPUT BUFFER
DQ
205
781
216
236
2 BIT-COLUMN PREFETCH
CAO
234
SENSE AMPS
16
DATA INPUT BUFFER/REG SERIAL TO PARALLEL
242
32
8192x256x32
8192x256x32
8192x256x32
8192x256x32
232
238
i DQS
i CK
CAD
ROW DECODER
222
210
REFRESH COUNTER ROW BUFFER
218
i AUTO REF
i RAS
BANK SELECT
224
212
ADDRESS REGISTER
214
202
CLK
206
ADD
204
BA0-1

FIG 7B


781
UDQS
LDQS
214
STROBE GEN
DLL
CLK
208
262
222
i_{DM}
UDM,LDM
207
COLUMN DECODER
226
LATENCY AND BURST LENGTH
MODE REGISTER
i_{MRS}
205
780
272
COMMAND SERIALIZER
TIMING REGISTER
WE
CAS
RAS
203
COLUMN BUFFER
220
i_{CAS}
CS
201
i_{WE}
$i_{AUTO\ REF}$
CKE
i_{RAS}
CLK
202
i_{CKE}

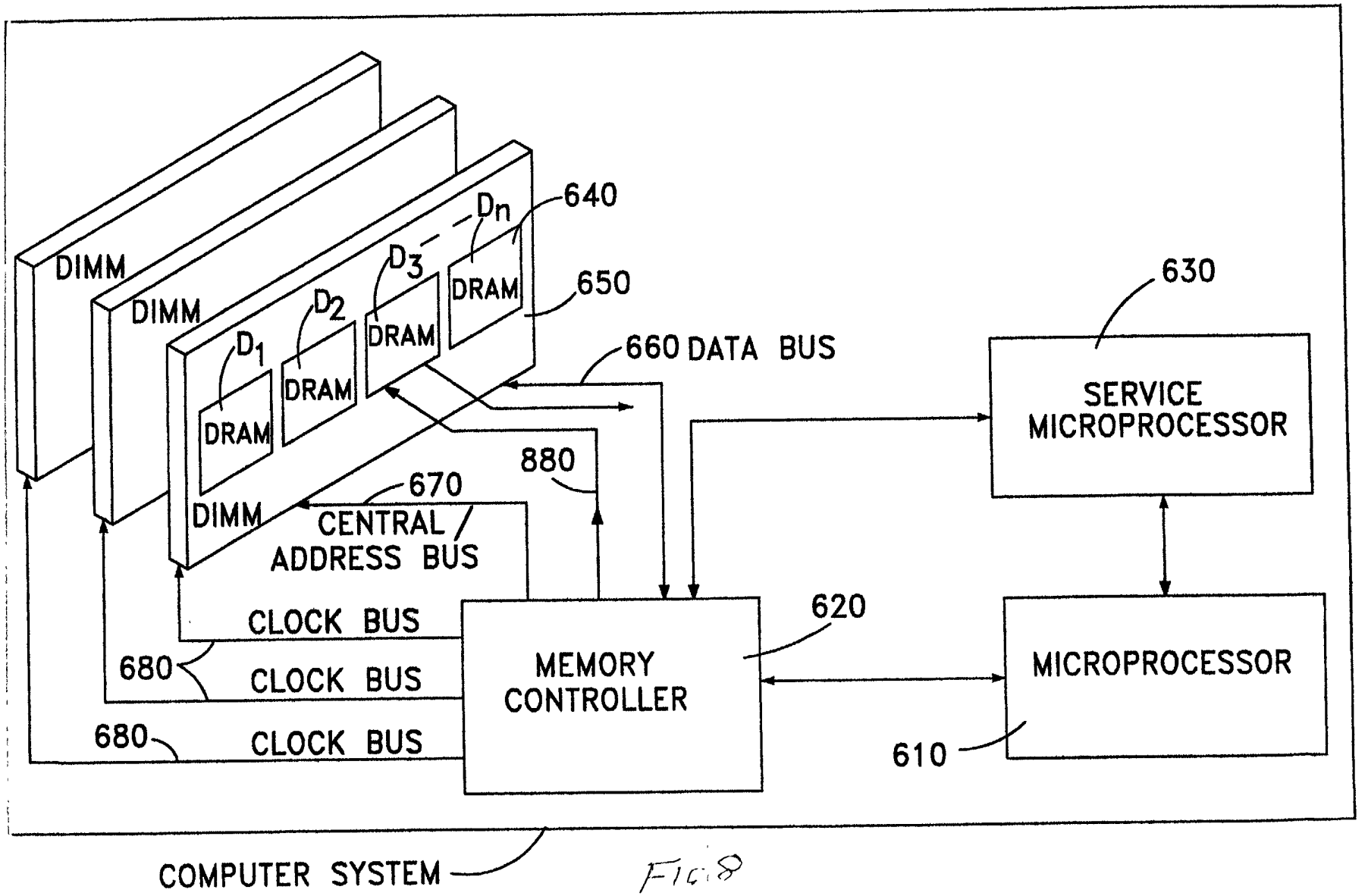
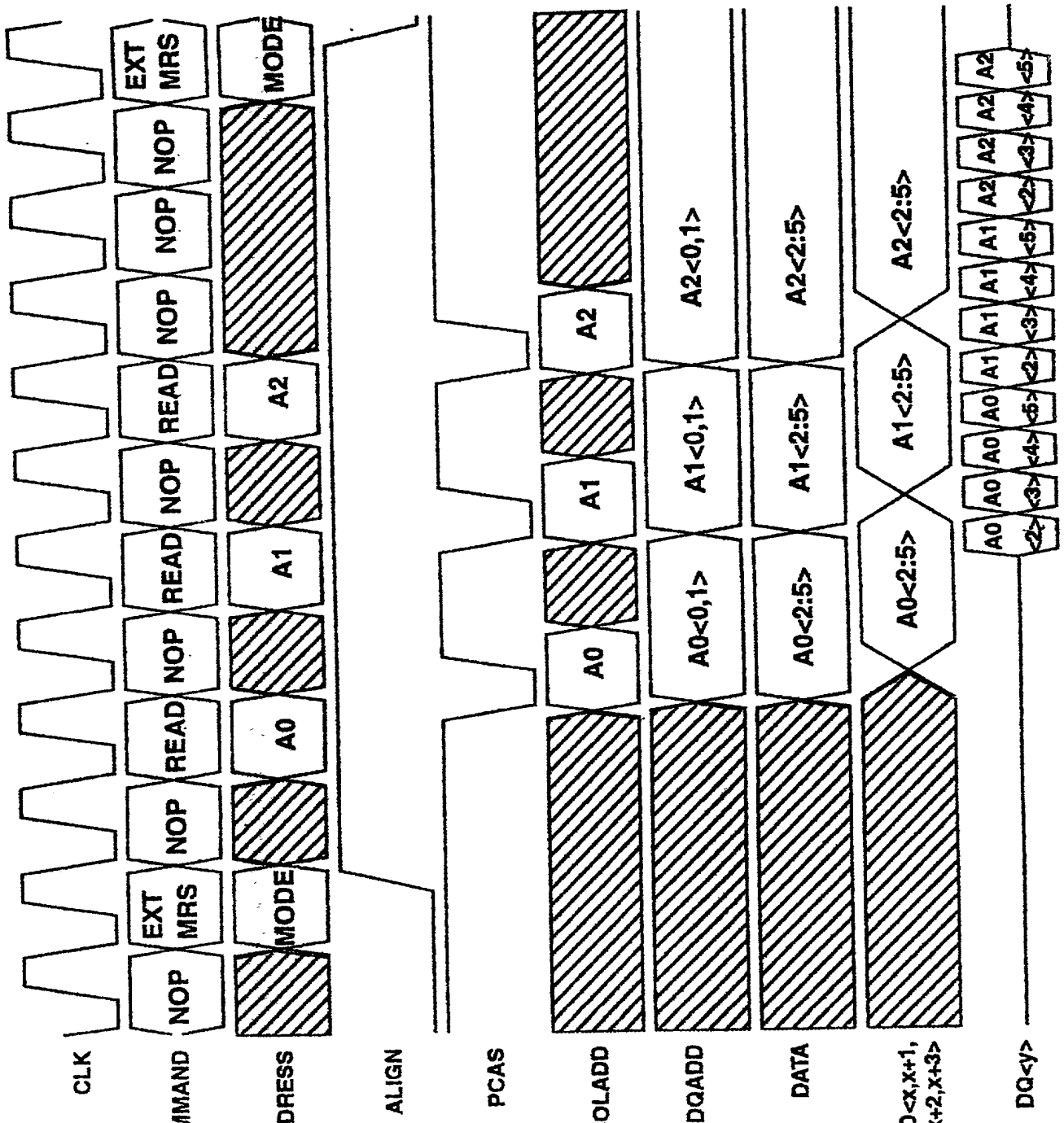


Fig 8

FIG. 9


CLK
COMMAND
ADDRESS
ALIGN
PCAS
COLADD
DQADD
DATA
RWD<x,x+1, x+2,x+3>
DQ<y>
NOP
EXT MRS
NOP
READ
NOP
READ
NOP
NOP
NOP
NOP
MODE
MODE
A0
A1
A2
A0
A1
A2
A0<0,1>
A1<0,1>
A2<0,1>
A0<2:5>
A1<2:5>
A2<2:5>
A0<2:5>
A1<2:5>
A2<2:5>
A0 A0 A0 A0 A0 A1 A1 A1 A1 A1 A2 A2 A2 A2 A2
<2> <3> <4> <5> <2> <3> <4> <5> <2> <3> <4> <5>

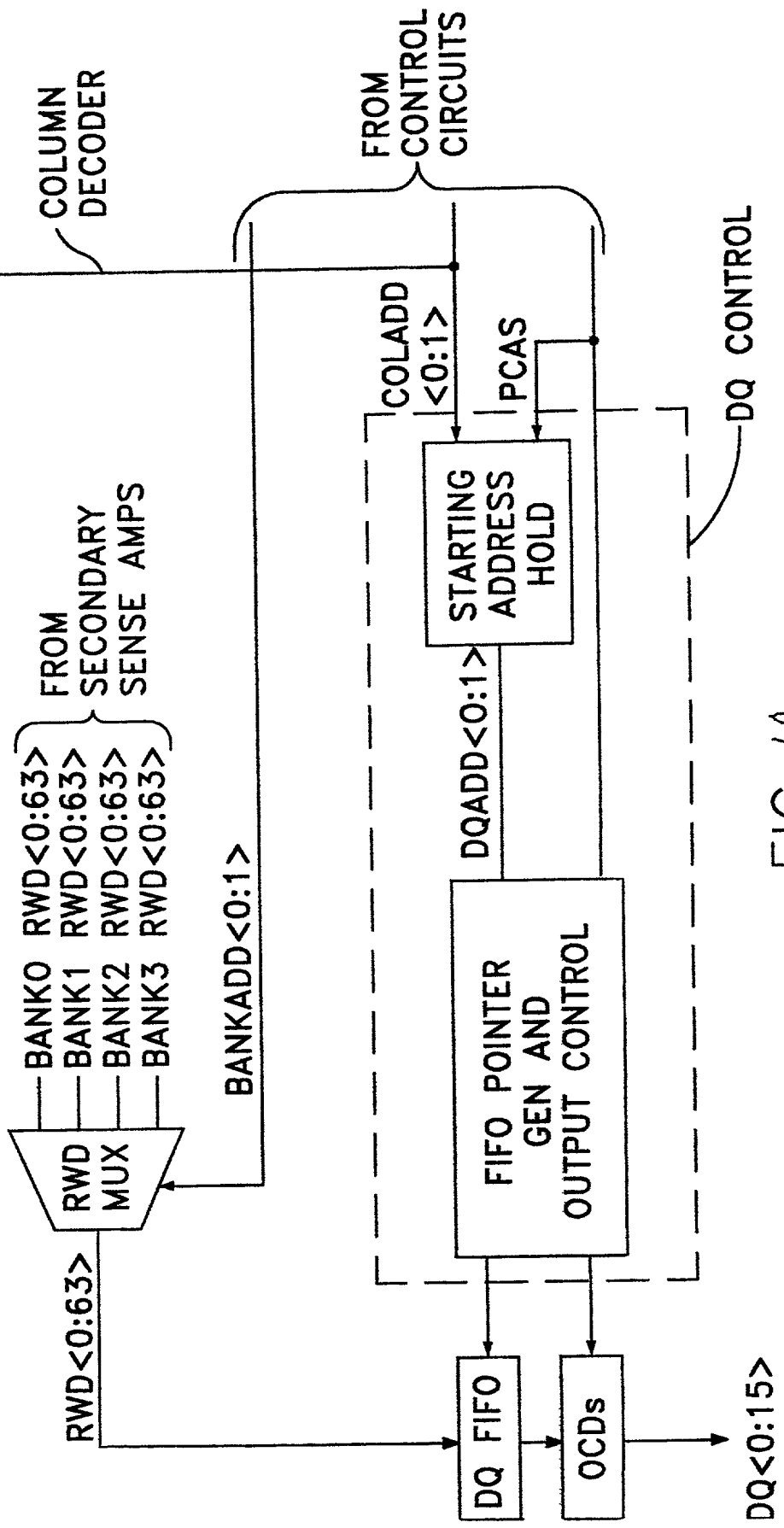

TO COLADD<0:1>
COLUMN DECODER
FROM CONTROL CIRCUITS
COLADD <0:1>
PCAS
DQ CONTROL
STARTING ADDRESS HOLD
DQADD<0:1>
FIFO POINTER GEN AND OUTPUT CONTROL
FROM SECONDARY SENSE AMPS
BANK0 RWD<0:63>
BANK1 RWD<0:63>
BANK2 RWD<0:63>
BANK3 RWD<0:63>
BANKADD<0:1>
RWD MUX
RWD<0:63>
DQ FIFO
OCDs
DQ<0:15>

FIG. 10

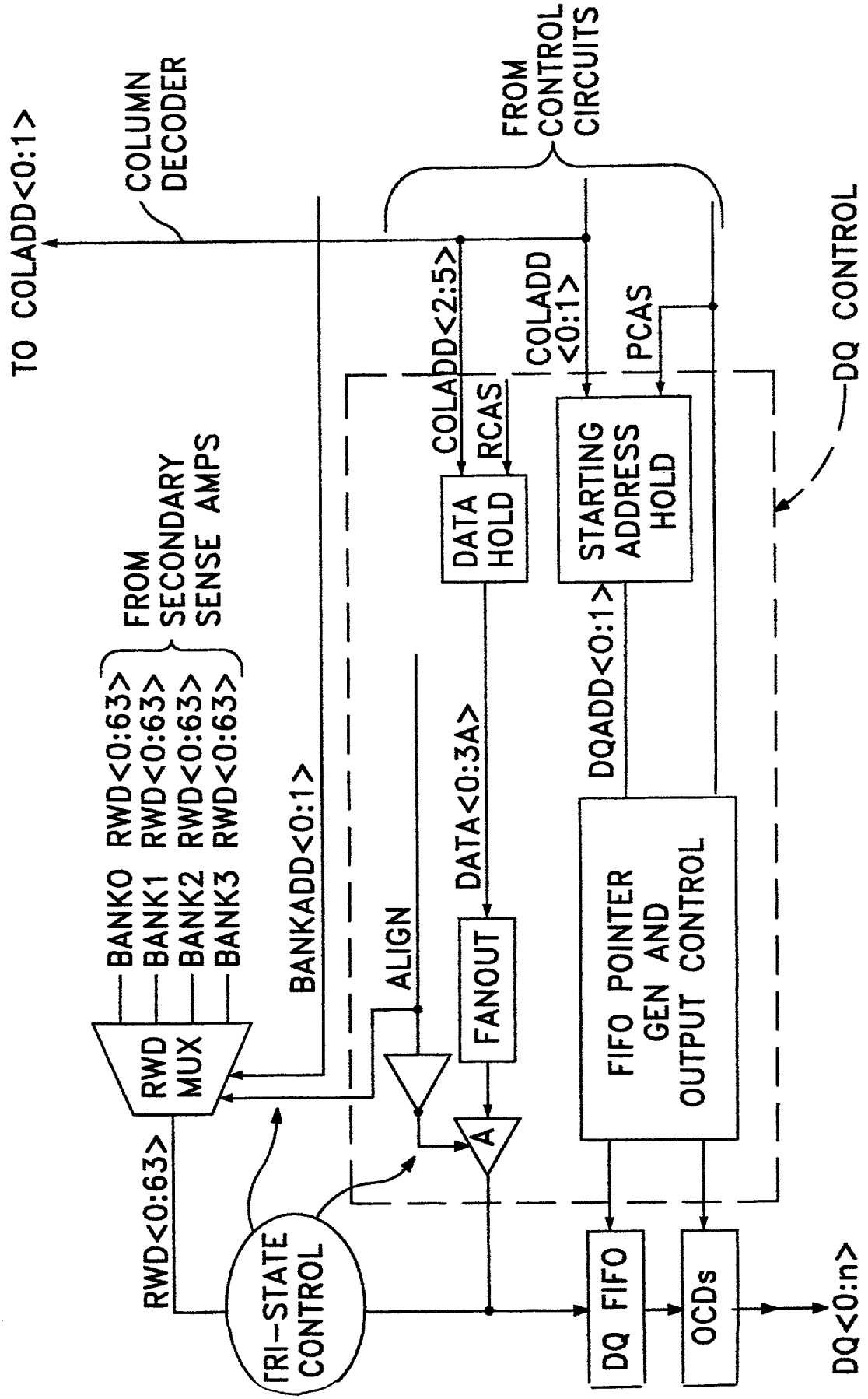
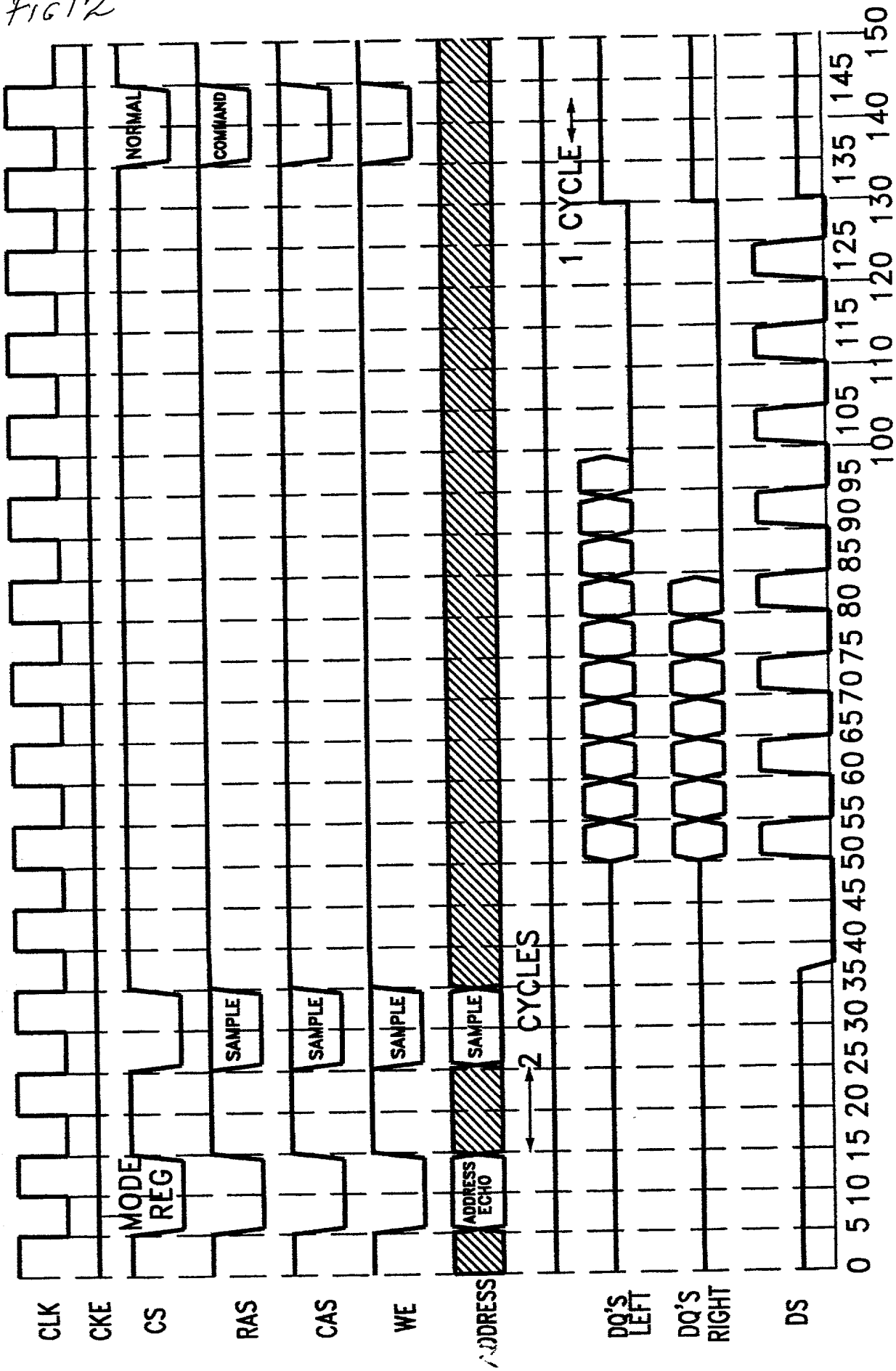

TO COLADD<0:1>
COLUMN DECODER
FROM CONTROL CIRCUITS
FROM SECONDARY SENSE AMPS
BANK0 RWD<0:63>
BANK1 RWD<0:63>
BANK2 RWD<0:63>
BANK3 RWD<0:63>
BANKADD<0:1>
COLADD<2:5>
RCAS
COLADD <0:1>
PCAS
DQ CONTROL
DATA HOLD
STARTING ADDRESS HOLD
ALIGN
DATA<0:3A>
DQADD<0:1>
RWD MUX
FANOUT
FIFO POINTER GEN AND OUTPUT CONTROL
A
RWD<0:63>
TRI-STATE CONTROL
DQ FIFO
OCDs
DQ<0:n>

FIG. 14

FIG 12


CLK
CKE
CS
RAS
CAS
WE
ADDRESS
DQ'S LEFT
DQ'S RIGHT
DS
MODE REG
NORMAL
COMMAND
SAMPLE
ADDRESS ECHO
2 CYCLES
1 CYCLE
0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145 150